IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Issue No.:	7,737,051
Issue Date:	June 15, 2010
Serial No.:	10/797,876
Filing Date:	March 10, 2004
Applicant:	Dip et al.
Title:	**SILICON GERMANIUM SURFACE LAYER FOR HIGH-K DIELECTRIC INTEGRATION**
Attorney Docket:	TPS-007
Confirmation No.:	5070

Cincinnati, Ohio 45202 August 27, 2010

VIA ELECTRONIC FILING
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

LETTER MAKING ERRORS OF RECORD

It is respectfully requested that this letter calling attention to the following errors in the specification in the above-identified patent be placed in the file wrapper history to make these errors of record.

In column 1, line 7, "processing, and more particularly," should read -- processing and, more particularly,--.

In column 7, line 32, "device be advantageous" should read -- device may be advantageous --.

In column 9, line 3, Claim 18, "providing a Si_substrate" should read --providing a Si substrate--.

Respectfully submitted,

WOOD, HERRON & EVANS, L.L.P.

By: /Kristi L. Davidson/
Kristi L. Davidson, Reg. No. 44,643

2700 Carew Tower
441 Vine Street
Cincinnati, OH 45202
(513) 241-2324 (voice)
(513) 241-6234 (facsimile)
kdavidson@whepatent.com
1232381v1